In the Claims:

Claims **1 to 28** (canceled).

29. (new) A single semiconductor element in a flip chip construction, comprising

a substrate layer at a rear side of the single semiconductor element;

an active layer which is arranged between the substrate layer and a contact side of the single semiconductor element disposed opposite the rear side; and

at least two solder contacts which are electrically connected to the active layer and project beyond the contact side of the single semiconductor element to enable a direct soldering of the single semiconductor element to a carrier board;

wherein the solder contacts respectively have different peripheral outlines, and the solder contacts respectively have at least one of: (a) the same peripheral length of the respective outlines or (b) the same surface area in comparison to one another, at the contact side of the single semiconductor element.

30. (new) The single semiconductor element in accordance with claim 29, wherein the respective outlines of the solder contacts have different shapes in comparison to one another.

31. (new) The single semiconductor element in accordance with claim 29, wherein the solder contacts respectively have the same surface area in comparison to one another at the contact side.

32. (new) The single semiconductor element in accordance with claim 31, wherein the respective outlines of the solder contacts respectively have the same peripheral length at the contact side.

33. (new) The single semiconductor element in accordance with claim 29, wherein the respective outlines of the solder contacts respectively have the same peripheral length at the contact side.

34. (new) The single semiconductor element in accordance with claim 29, further comprising at least one dummy contact in addition to the solder contacts to increase the standing stability.

35. (new) The single semiconductor element in accordance with claim 29, wherein at least one of the solder contacts includes a plurality of contact parts at the contact side of the single semiconductor element.

36. (new) The single semiconductor element in accordance with claim 29, wherein at least one of the solder contacts

extends along at least two outer edges of the contact side of the single semiconductor element.

37. (new) The single semiconductor element in accordance with claim 29, wherein at least one of the solder contacts extends along at least three outer edges of the contact side of the single semiconductor element.

38. (new) The single semiconductor element in accordance with claim 29, wherein the outline of a first one of the solder contacts is a circular outline and the outline of a second one of the solder contacts is an elongate outline.

39. (new) The single semiconductor element in accordance with claim 29,

wherein the outline of a first one of the solder contacts is a U-shaped or C-shaped outline and extends along three outer edges of the contact side (23) of the single semiconductor element; and

wherein the outline of a second one of the solder contacts is at least partly enclosed inside the U-shaped or C-shaped outline of the first solder contact.

40. (new) The single semiconductor element in accordance with claim 29, further comprising a glass passivation layer that peripherally surrounds the solder contacts on the contact side.

41. (new) The single semiconductor element in accordance with claim 40, wherein the glass passivation layer is interrupted in a region of the solder contacts and in a region of a dividing grid between a plurality of said single semiconductor elements produced adjacent to one another.

42. (new) The single semiconductor element in accordance with claim 40, further comprising an oxide layer provided between the glass passivation layer and the active layer.

43. (new) The single semiconductor element in accordance with claim 40, further comprising an intermediate metal layer by which the solder contacts are connected to the active layer.

44. (new) A method for producing the single semiconductor element in accordance with claim 40 in a flip chip construction, the method comprising the steps of:

a) providing the active layer on the substrate layer;

b) producing and electrically connecting the solder contacts to the active layer; and

c) before or after producing the solder contacts, providing a glass passivation layer that peripherally surrounds the contacts;

wherein the step of providing the glass passivation layer comprises the sub-steps of:

c1) wetting the contact side with a suspension such that glass particles contained therein are deposited at the contact side due to gravity or due to a centrifugal force; and

c2) subsequently heating the contact side to fuse the deposited glass particles.

45. (new) The method in accordance with claim 44, wherein the step c) involves first providing the glass passivation layer over the whole area of the contact side and then photolithographically patterning the glass passivation layer so that the contact side is liberated from the glass passivation layer in the region of the solder contacts.

46. (new) The method in accordance with claim 44, wherein

the single semiconductor element is produced together with a plurality of other single semiconductor elements on a common substrate,

the contact sides of the single semiconductor elements are kept free or liberated from the glass passivation layer along a dividing grid, and

the single semiconductor elements are sawn apart along the dividing grid.

47. (new) The single semiconductor element in accordance with claim 29, further comprising an insulator layer provided on at least a portion of at least one side face of the single semiconductor element.

48. (new) The single semiconductor element in accordance with claim 47, wherein at least a quarter of the side face of the single semiconductor element adjoining the contact side is provided with the insulator layer.

49. (new) The single semiconductor element in accordance with claim 47, wherein the entirety of the side face of the single semiconductor element is provided with the insulator layer.

50. (new) The single semiconductor element in accordance with claim 47, wherein the single semiconductor element has a mesa construction with lateral etched and sawn-through trenches, with the respective side face being provided with the insulator layer down to the depth of the respective trench.

51. (new) The single semiconductor element in accordance with claim 47,

wherein at least the side faces of the single semiconductor element which respectively directly adjoin a solder contact are provided with the insulator layer;

wherein in particular all side faces of the single semiconductor element are provided with the insulator layer.

52. (new) The single semiconductor element in accordance with claim 47, wherein the contact side is also provided with the insulator layer.

53. (new) The single semiconductor element in accordance with claim 47, wherein the insulator layer is an oxide layer.

54. (new) A method for producing a plurality of single semiconductor elements in accordance with claim 47, wherein

for the preparation of a plurality of the adjacent single semiconductor elements, a substrate is provided with a respective active layer and with dividing trenches lying therebetween;

the active layers and the dividing trenches lying therebetween are provided with an insulator layer; and

the adjacent single semiconductor elements are sawn apart along the dividing trenches.

55. (new) The method in accordance with claim 54, wherein the insulator layer is an oxide layer.

56. (new) The method in accordance with claim 54, wherein the insulator layer is applied in a CVD process.

[RESPONSE CONTINUES ON NEXT PAGE]